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(71) Applicant: **NEC CORPORATION**
Tokyo (JP)

(72) Inventor:
Yamaguchi, Michimasa,
c/o NEC IC Microcomputer
Kawasaki-shi, Kanagawa (JP)

(74) Representative: **Betten & Resch**
Reichenbachstrasse 19
80469 München (DE)

(54) Frequency measurement test circuit and semiconductor integrated circuit having the same

(57) A frequency measurement test circuit includes a frequency divider, and a detection circuit. The frequency divider frequency-divides an input to be measured. The detection circuit outputs a signal of level set on the basis of a relationship in magnitude between the frequency of the signal frequency-divided by the frequency divider and that of a reference clock signal.

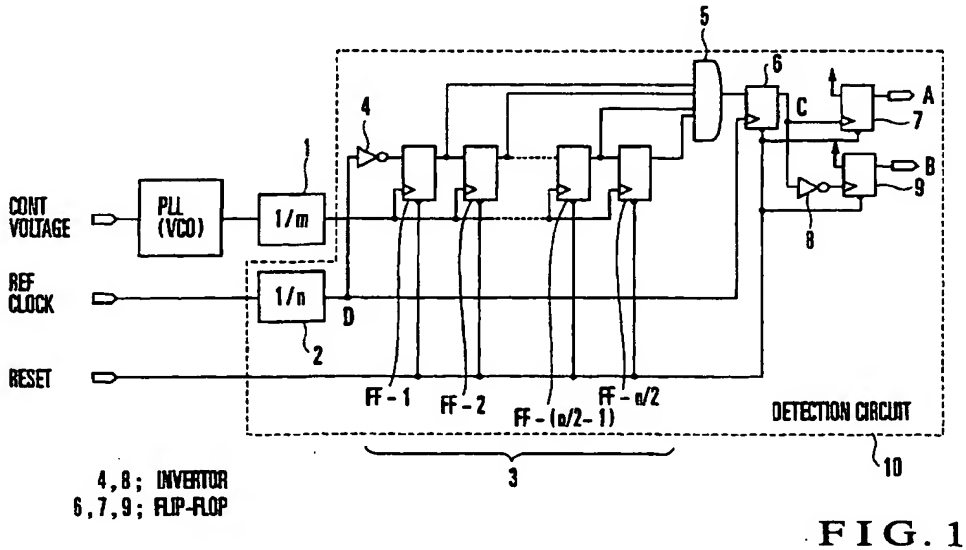

FIG. 1

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Description

Background of the Invention

[0001] The present invention relates to a frequency measurement test circuit used to measure the frequency of a signal output from, e.g., a phase-locked loop incorporated in a large scale integrated circuit, and a semiconductor integrated circuit having the frequency measurement test circuit.

[0002] Conventionally, to test a large scale integrated circuit (to be referred to as an LSI hereinafter) incorporating a phase-locked loop (to be referred to as a PLL hereinafter), generally, the frequency in the locked state of the PLL is measured using an analog tester and digital tester, and it is checked whether the frequency has a desired value. That is, testing need be performed twice with the analog tester and digital tester. However, the analog tester and digital tester are expensive, and the measurement time is long because measurement must be performed twice. An apparatus capable of testing frequencies using only a digital tester has been disclosed.

[0003] Figs. 3A and 3B show conventional test circuit. As shown in Figs. 3A and 3B, conventional digital testers (test circuits) 11a and 11b are arranged outside digital integrated circuits (to be referred to as ICs hereinafter) 12 each incorporating a PLL. The digital testers 11a and 11b have external and internal frequency measurement devices 13a and 13b, respectively. The frequency measurement device 13a or 13b measures the frequency in the locked state of the PLL. The digital tester 11a or 11b determines whether the measured frequency has a desired value. Since such conventional digital tester 11a or 11b requires the frequency measurement device 13a or 13b, the circuit becomes complex. Japanese Patent Laid-Open No. 9-197024 has proposed a simple and inexpensive test circuit that solves the problem.

[0004] Fig. 4 shows the conventional test circuit disclosed in Japanese Patent Laid-Open No. 9-197024. The conventional test circuit disclosed in this prior art has two counters 22a and 22b which receive a signal output from a PLL 21. The two counters 22a and 22b are selected by a control signal CE whose duty ratio is 50%. The test circuit also has a comparator 23 for comparing the signal output from the counter 22a within a predetermined period with that output from the counter 22b within a predetermined period. The test circuit further has a decoder 24 for outputting a signal in association with the output signals from the counters 22a and 22b and comparator 23.

[0005] This conventional test circuit requires no frequency measurement device, and the circuit is simple. Since testing can be performed using only one tester, the circuit is less expensive than conventional circuits. However, the conventional test circuit disclosed in the above prior art requires the two counters 22a and 22b to detect that the phase is locked in the PLL 21. Hence, the measurement accuracy must be increased by prolonging the measurement time. However, to prolong the measurement time, the counters 22a and 22b must have a large circuit scale. In addition, since the duty ratio of the control signal CE for controlling the counters 22a and 22b must be 50%, very high accuracy is required. To solve these problems, a circuit for detecting the phase-locked state is generally provided in the PLL.

[0006] Recently, a demand has arisen for measurement of not only the frequency of the PLL but also the oscillation frequency of a voltage-controlled oscillator (to be referred to as a VCO hereinafter) incorporated in the IC. The above-described circuit that receives the lock detection signal from the PLL can measure only the frequency in the phase-locked state of the PLL.

Summary of the Invention

[0007] The present invention has been made in consideration of the above problems, and has as its object to provide a frequency measurement test circuit capable of accurately measuring a frequency whose phase is not locked, and a semiconductor integrated circuit having the frequency measurement test circuit.

[0008] In order to achieve the above object, according to the present invention, there is provided a frequency measurement test circuit comprising a frequency divider for frequency-dividing an input to be measured, and a detection circuit for outputting a signal of level set on the basis of a relationship in magnitude between the frequency of the signal frequency-divided by the frequency divider and that of a reference clock signal.

Brief Description of the Drawings

[0009]

Fig. 1 is a block diagram showing the arrangement of a frequency measurement test circuit according to an embodiment of the present invention;

Figs. 2A, 2B, and 2C are timing charts showing operation of the frequency measurement test circuit according to the embodiment of the present invention;

Figs. 3A and 3B are block diagrams showing conventional test circuits; and

Fig. 4 is a block diagram showing a conventional test circuit disclosed in Japanese Patent Laid-Open No. 9-197024.

Description of the Preferred Embodiment

[0010] A test circuit according to an embodiment of the present invention will be described below in detail with reference to the accompanying drawings.

[0011] Fig. 1 shows the arrangement of a frequency

measurement test circuit according to an embodiment of the present invention. The circuit of this embodiment has a frequency divider 1 for receiving the output signal from a phase-locked loop (PLL) or a voltage-controlled oscillator (VCO) that receives a constant voltage. The frequency divider 1 divides the frequency of the input signal to 1/m. That is, the frequency of the signal from the PLL or VCO is multiplied by 1/m by the frequency divider 1. The circuit also has a frequency divider 2 that receives a reference clock signal. The frequency divider 2 divides the frequency of the input signal to 1/n. That is, the frequency of the reference clock signal is multiplied by 1/n by the frequency divider 2, where n must always be an even value.

[0012] The circuit further has a shift register 3 constructed by n/2 flip-flops FF-1 to FF-n/2. The output terminal of the frequency divider 1 is connected to the clock signal input terminals of the flip-flops FF-1 to FF-n/2. In the shift register 3, every time the output signal from the frequency divider 1 changes from "0" to "1", data in the shift register 3 shifts to the output side by one stage. An inverter 4 is connected to the output terminal of the frequency divider 2. The output terminal of the inverter 4 is connected to the data input terminal of the flip-flop FF-1 located at the first stage of the shift register 3 having n/2 stages. The test circuit also has an AND circuit 5 for ANDing signals from all the output terminals of the 2/n flip-flops FF-1 to FF-n/2 of the shift register 3.

[0013] The test circuit further has a flip-flop 6 having a data input terminal connected to the output terminal of the AND circuit 5. The output terminal of the frequency divider 2 is also connected to the clock input terminal of the flip-flop 6. The test circuit also has a flip-flop 7 having a clock input terminal connected to the output terminal of the flip-flop 6 and an inverter 8 having an input terminal connected to the output terminal of the flip-flop 6. The output terminal of the inverter 8 is connected to the clock input terminal of a flip-flop 9. The data input terminals of the flip-flops 7 and 9 are fixed at "1" level. When the output signal from the flip-flop 6 changes from "0" to "1", the output signal from the flip-flop 7 changes from "1" to "0". When the output signal from the flip-flop 6 changes from "1" to "0", the output signal from the flip-flop 9 changes from "0" to "1". For this reason, it can be detected that the output signal from the flip-flop 6 has changed from "0" to "1" or from "1" to "0". A reset supply terminal to which a reset signal is supplied is connected to the reset input terminals of all the flip-flops. The frequency divider 2, shift register 3, inverters 4 and 8, AND circuit 5, and flip-flops 6, 7, and 9 constitute a detection circuit 10 for outputting a signal of level set on the basis of the relationship in magnitude between the frequency of the signal frequency-divided by the frequency divider 1 and that of the reference clock signal.

[0014] The operation of this embodiment having the above-described arrangement will be described next. Before inspecting the frequency, "0" is input to the reset signal when a signal from the PLL or VCO and the reference clock signal are being supplied, thereby resetting all the flip-flops. With this operation, all bits of the shift register 3 and all the output signals from the AND circuit 5 and flip-flops 6, 7, and 9 become "0".

[0015] Inspection is started by changing the reset signal from "0" to "1". When the output signal from the frequency divider 2 is "0", the input value to the first flip-flop FF-1 of the shift register 3 is "1". In this state, when the output signal from the frequency divider 1 changes from "0" to "1", the input value "1" to the first flip-flop FF-1 of the shift register 3 is input to the second flip-flop FF-2. When the output signal from the frequency divider 1 changes from "0" to "1" again, the input value "1" to the first and second flip-flops FF-1 and FF-2 of the shift register 3 is input to the third flip-flop. In this way, every time the output from the frequency divider 1 changes from "0" to "1" while the output from the frequency divider 2 is being "0", the input value "1" is shifted to the next stage in the shift register 3.

[0016] In this embodiment, all the output terminals of the bits of the shift register 3 are connected to the AND circuit 5. When all the output values from the flip-flops in the shift register 3 become "1" as the result of the above-described shift, the output from the AND circuit 5 is "1". Otherwise, the output from the AND circuit 5 remains "0". After this, when the output signal from the frequency divider 2 changes from "0" to "1", the flip-flop 6 receives the output signal from the AND circuit 5 and outputs the signal to the flip-flops 7 and 9. At this time, when the output signal from the flip-flop 6 changes from "0" to "1", the output signal from the flip-flop 7 changes to "1". When the output signal from the flip-flop 6 changes from "1" to "0", the output signal from the flip-flop 9 changes to "1". Let X (Hz) be the frequency of the signal output from the PLL or VCO, and Y (Hz) be the frequency of the reference clock signal. The outputs from the flip-flops 7 and 9 change depending on the relationship in magnitude between $(X \div m)$ and Y.

[0017] Figs. 2A, 2B, and 2C show the operation of the frequency measurement test circuit according to the embodiment of the present invention. Fig. 2A shows a case wherein $(X \div m) \geq Y$ holds. Fig. 2B shows a case wherein $(X \div m) < Y$ holds, and the difference is small. Fig. 2C shows a case wherein $(X \div m) < Y$ holds, and the difference is large.

[0018] When $(X \div m) \geq Y$ holds (case 1), the output signal from the frequency divider 1 changes from "0" to "1" n/2 times or more while the output signal from the frequency divider 2 is being "0". For this reason, all bits of the shift register 3 having n/2 stages are fixed at "1". As shown in Fig. 2A, the output signal from the AND circuit 5 is "1". When the output signal from the frequency divider 2 changes from "0" to "1", the output signal from the flip-flop 6 changes from "0" to "1". Consequently, the output from the flip-flop 7 is fixed at "1", and the output signal from the flip-flop 9 is fixed at "0".

[0019] Two situations are assumed when $(X \div m) <$

Y holds. As one situation, the difference between (X ÷ m) and Y is small, and the output signal from the frequency divider 1 changes from "0" to "1" n/2 times or a number of times less than n/2 while the output signal from the frequency divider 2 is being "0". As the other situation, the difference between (X ÷ m) and Y is large, and the output signal from the frequency divider 1 always changes from "0" to "1" a number of times less than n/2 while the output signal from the frequency divider 2 is being "0".

[0020] Assume that the difference between (X ÷ m) and Y is small, and the output signal from the frequency divider 1 changes from "0" to "1" n/2 times or a number of times less than n/2 while the output signal from the frequency divider 2 is being "0" (case 2). In this case, as shown in Fig. 2B, when the output signal from the frequency divider 1 changes from "0" to "1" n/2 times, the same operation as that when (X ÷ m) ≧ Y holds is performed. For this reason, when the output signal from the frequency divider 2 changes from "0" to "1", the output signal from the flip-flop 6 is "1".

[0021] When the output signal from the frequency divider 1 changes from "0" to "1" a number of times less than n/2, the output signal from the frequency divider 2 changes from "0" to "1" before all bits of the shift register 3 change to "1". For this reason, when the output signal from the frequency divider 2 changes from "0" to "1", the output signal from the flip-flop 6 is "0".

[0022] Fig. 2B shows an operation when the output from the frequency divider 1 changes n/2 times in the first and third changes in the output signal from the frequency divider 2 from "0" to "1", and the output from the frequency divider 2 changes a number of times less than n/2 in the second change. In the operation shown in Fig. 2B, when the output signal from the frequency divider 2 changes from "0" to "1" for the first time, the output signal from the flip-flop 7 is "1", and the output signal from the flip-flop 9 is "0". After this, when the output signal from the frequency divider 2 changes from "0" to "1" for the second time, the output signal from the flip-flop 6 changes from "1" to "0. For this reason, the output signal from the flip-flop 9 changes from "0" to "1". However, the output signal from the flip-flop 7 remains "1".

[0023] When the output signal from the frequency divider 2 changes from "0" to "1" for the third time, the output signal from the flip-flop 6 changes from "0" to "1". However, the output signals from the flip-flops 7 and 9 are already "1" and remain "1". Finally, the output signal from the flip-flop 7 is fixed at "1", and the output signal from the flip-flop 9 is also fixed at "1".

[0024] Assume that the difference between (X ÷ m) and Y is large, and the output signal from the frequency divider 1 always changes from "0" to "1" a number of times less than n/2 while the output signal from the frequency divider 2 is being "0" (case 3). In this case, several bits of the shift register 3 are always "0". For this reason, the output signal from the frequency divider 2 changes from "0" to "1" before all bits of the shift register 3 change to "1", as shown in Fig. 2C. As a consequence, even when the output signal from the frequency divider 2 changes from "0" to "1", the output signal from the flip-flop 6 remains "0". Hence, the output signals from the flip-flops 7 and 9 also remain "0". For this reason, the output signals from the flip-flops 7 and 9 are fixed at "0".

[0025] According to the this embodiment, the finally fixed values of the output signals from the flip-flops 7 and 9 change depending on the relationship in magnitude between (X ÷ m) and Y. More specifically, in case 1, the output signal from the flip-flop 7 is fixed at "1", and the output signal from the flip-flop 9 is fixed at "0". In case 2, both the output signals from the flip-flops 7 and 9 are fixed at "1". In case 3, both the output signals from the flip-flops 7 and 9 are fixed at "0".

[0026] When the output signal from the flip-flop 7 is fixed at "1", and the output signal from the flip-flop 9 is fixed at "0", the frequency of the output signal from the PLL or VCO has a value equal to or larger than that obtained by multiplying the frequency of the reference clock signal by m. When both the output signals from the flip-flops 7 and 9 are fixed at "1", the frequency of the output signal from the PLL or VCO has a value smaller than that obtained by multiplying the frequency of the reference clock signal by m, and the difference between the frequencies is small. When both the output signals from the flip-flops 7 and 9 are fixed at "0", the frequency of the output signal from the PLL or VCO has a value smaller than that obtained by multiplying the frequency of the reference clock signal by m, and the difference between the frequencies is large.

[0027] A method of measuring a frequency with a tester using an LSI incorporating the test circuit of this embodiment will be described next. Normally, a tester uses a test pattern, and an input waveform and output expectation value are described in the test pattern. In this embodiment, the reference clock used in the test circuit is input from the tester to the LSI, and the test result by the test circuit is received from the LSI to the tester and compared with the expectation value prepared in the test pattern, thereby obtaining the relationship between the reference clock and the oscillation frequency of the PLL or VCO.

[0028] In the case to be described below, a value output from the LSI when the value obtained by dividing the oscillation frequency of the PLL or VCO by m is equal to or larger than the reference clock is described as the expectation value. That is, the state wherein the output signal from the flip-flop 7 is finally fixed at "1", and the output signal from the flip-flop 9 is "0" is described as the expectation value.

[0029] First, the frequency of the reference clock signal is set at Z_1 (Hz), and testing is performed. If the output value does not coincide with the expectation value, the value obtained by multiplying the oscillation frequency of the PLL or VCO by m is smaller than the value of the operating frequency of the reference clock

signal. When the output value coincides with the expectation value, the value obtained by multiplying the oscillation frequency of the PLL or VCO by m is equal to or larger than the value of the operating frequency of the reference clock signal.

[0030] Next, the frequency of the reference clock signal is set at Z_2 (Hz), and the same testing as described above is performed. When the output value for the frequency set at Z_1 (Hz) coincides with the expectation value, testing is performed assuming that $Z_2 > Z_1$. When the output value for the frequency set at Z_1 (Hz) does not coincide with the expectation value, testing is performed assuming that $Z_2 < Z_1$. Under this condition, the relationship between the reference clock signal and the oscillation frequency of the PLL or VCO is obtained.

[0031] When the operating frequency of the reference clock signal is repeatedly changed in the above-described manner, the maximum frequency of the reference clock signal for which the output value coincides with the expectation value can be obtained. Letting Z_x (Hz) be the frequency of the reference clock, the oscillation frequency of the PLL or VCO is given by ($Z_x \times m$) (Hz), and the oscillation frequency of the PLL or VCO can be reliably obtained. When it is to be checked using the tester whether the oscillation frequency of the PLL or VCO is higher (or lower) than a given frequency, the range matching with the expectation value need not be obtained, and only testing is performed once.

[0032] According to this embodiment, since measurement can be performed independently of the phase-locked state of the PLL, the test circuit can be used to test a single VCO. In addition, since no counter is required, the circuit scale is small. Furthermore, the frequency can be measured at a high accuracy. Since the frequency division value of the frequency divider can be changed, the test circuit can be easily adapted to various types of digital testers.

[0033] As has been described above, according to the present invention, a detection circuit for outputting different signals in association with the difference between the frequency of the signal frequency-divided by the frequency divider and that of the reference clock signal is prepared. Since the relationship in magnitude between the frequency and the reference clock signal can be obtained independently of the phase-locked state of the input signal to be measured, the test circuit can be used to test a voltage-controlled oscillator. Since no counter is required, the circuit scale can be made small, and the frequency can be accurately measured. Additionally, since the frequency division value of the frequency divider can be changed, the test circuit can be easily adapted to various types of digital testers. In the present invention, since the test circuit is incorporated, the oscillation frequency of a phase-locked loop or voltage-controlled oscillator can be measured.

Claims

1. A frequency measurement test circuit characterized by comprising:

   a frequency divider (1) for frequency-dividing an input to be measured; and
   a detection circuit (10) for outputting a signal of level set on the basis of a relationship in magnitude between the frequency of the signal frequency-divided by said frequency divider (1) and that of a reference clock signal.

2. A circuit according to claim 1, wherein

   said detection circuit (10) comprises a second frequency divider (2) for dividing the frequency of the reference clock signal to 1/n (n is a positive even number), an inverter (4) for inverting a signal output from said second frequency divider (2), a shift register (3) constructed by (n/2) series-connected flip-flops (FF-1 - FF-n/2) including a flip-flop (FF-1) at a first stage having a data input terminal connected to an output terminal of said inverter (4), and an AND circuit (5) for ANDing output signals from said flip-flops (FF-1 - FF-n/2).

3. A circuit according to claim 2, wherein

   said detection circuit (10) comprises a second flip-flop (6) having a data input terminal to which an output signal from said AND circuit (5) is input, and a clock input terminal to which a signal divided to 1/n by said second frequency divider (2) is input.

4. A circuit according to claim 3, wherein

   said detection circuit (10) comprises a third flip-flop circuit (7) having a clock input terminal to which an output signal from said second flip-flop (6) is input, and a data input terminal fixed at high level, a second inverter (8) for inverting the output signal from said second flip-flop (6), and a fourth flip-flop circuit (9) having a clock input terminal to which a signal output from said second inverter (8) is input, and a data input terminal fixed at high level.

5. A semiconductor integrated circuit characterized by comprising:

   a frequency measurement test circuit having a frequency divider (1) for frequency-dividing an input to be measured, and a detection circuit (10) for outputting a signal of level set on the basis of a relationship in magnitude between

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the frequency of the signal frequency-divided by said frequency divider (1) and that of a reference clock signal; and

a circuit (PLL, VCO) for outputting the signal to be measured.

6. A circuit according to claim 5, wherein

said detection circuit (10) comprises a second frequency divider (2) for dividing the frequency of the reference clock signal to 1/n (n is a positive even number), an inverter (4) for inverting a signal output from said second frequency divider (2), a shift register (3) constructed by (n/2) series-connected flip-flops (FF-1 - FF-n/2) including a flip-flop (FF-1) at a first stage having a data input terminal connected to an output terminal of said inverter (4), and an AND circuit (5) for ANDing output signals from said flip-flops (FF-1 - FF-n/2).

7. A circuit according to claim 6, wherein

said detection circuit (10) comprises a second flip-flop (6) having a data input terminal to which an output signal from said AND circuit (5) is input, and a clock input terminal to which a signal divided to 1/n by said second frequency divider (2) is input.

8. A circuit according to claim 7, wherein

said detection circuit (10) comprises a third flip-flop circuit (7) having a clock input terminal to which an output signal from said second flip-flop (6) is input, and a data input terminal fixed at high level, a second inverter (8) for inverting the output signal from said second flip-flop (6), and a fourth flip-flop circuit (9) having a clock input terminal to which a signal output from said second inverter (8) is input, and a data input terminal fixed at high level.

9. A circuit according to one of claims 5 to 8, wherein

said circuit or outputting the signal to be measured comprises a phase-locked loop (PLL).

10. A circuit according to one of claims 5 to 8, wherein

said circuit for outputting the signal to be measured comprises a voltage-controlled oscillator (VCO).

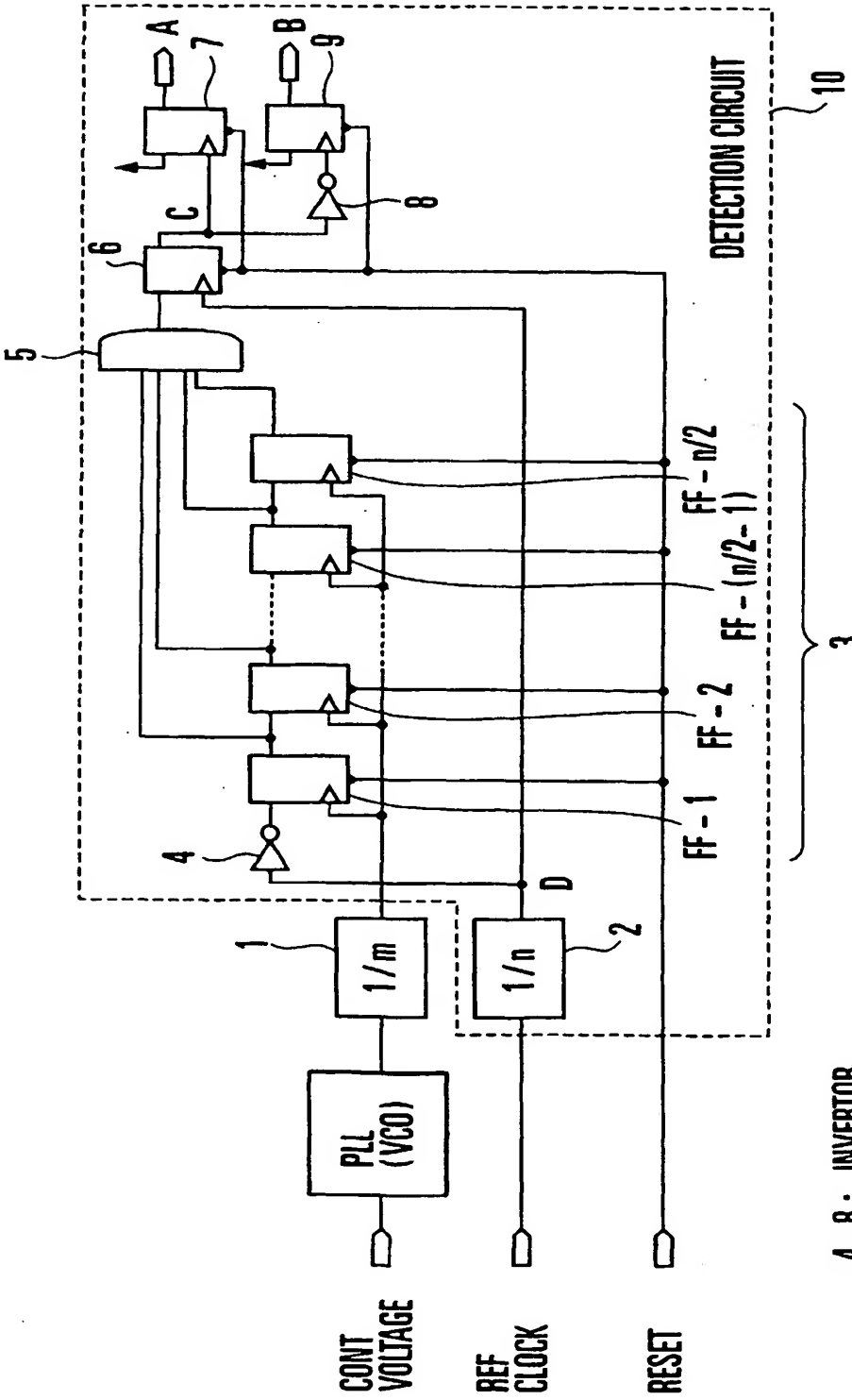
A
B
7
9
C
8
6
5
DETECTION CIRCUIT
10
FF-n/2
FF-(n/2-1)
FF-2
FF-1
3
4
D
1
1/m
1/n
2
PLL (VCO)
CONT VOLTAGE
REF CLOCK
RESET
4,8; INVERTOR
6,7,9; FLIP-FLOP

FIG. 1

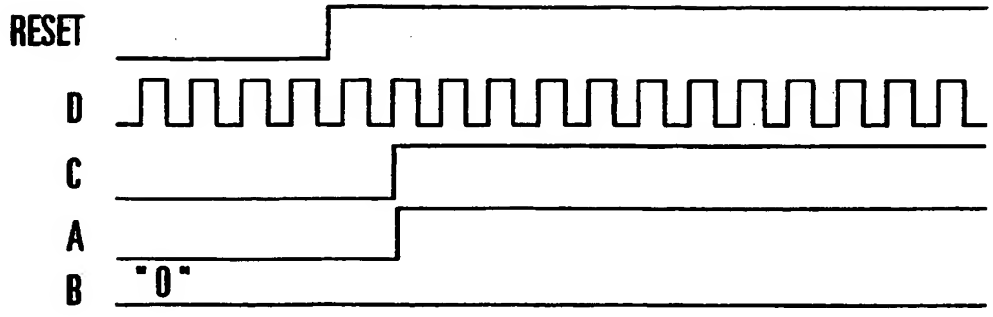

FIG. 2A

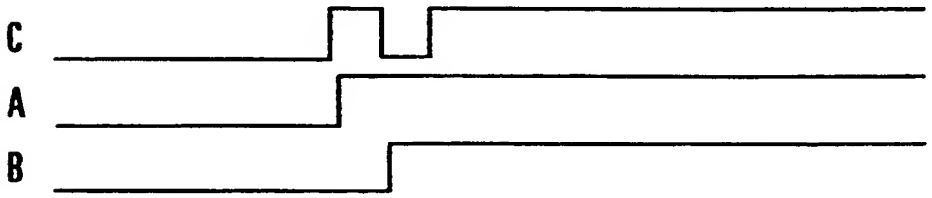

FIG. 2B

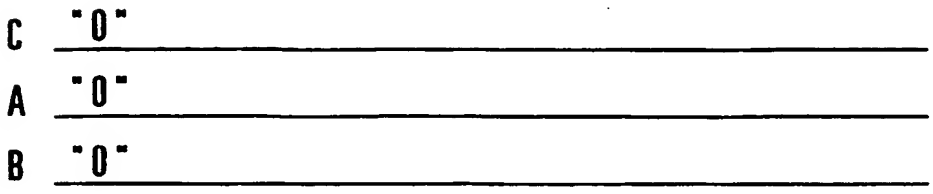

FIG. 2C

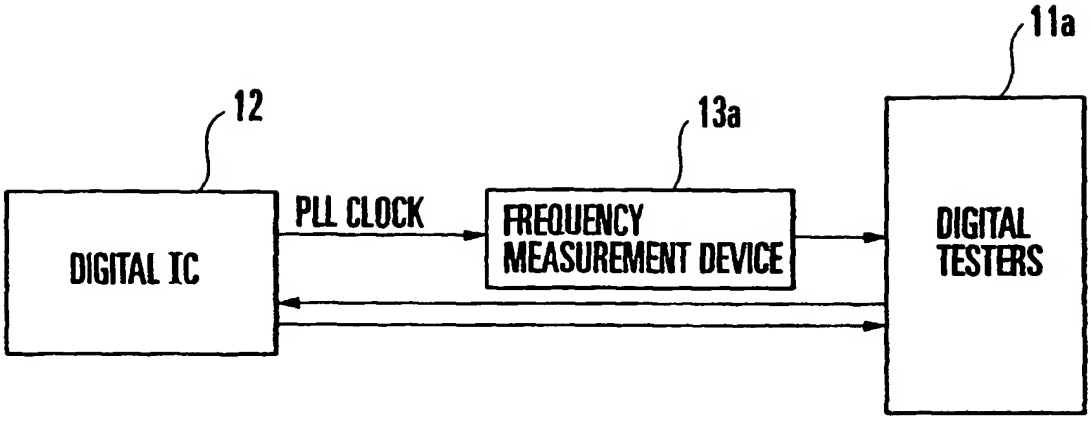
11a
12
13a
DIGITAL IC
PLL CLOCK
FREQUENCY MEASUREMENT DEVICE
DIGITAL TESTERS

FIG. 3A

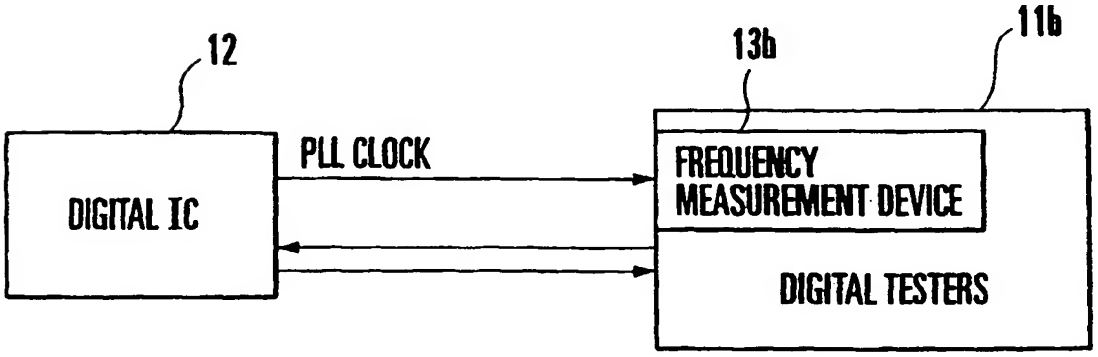
12
13b
11b
DIGITAL IC
PLL CLOCK
FREQUENCY MEASUREMENT DEVICE
DIGITAL TESTERS

FIG. 3B

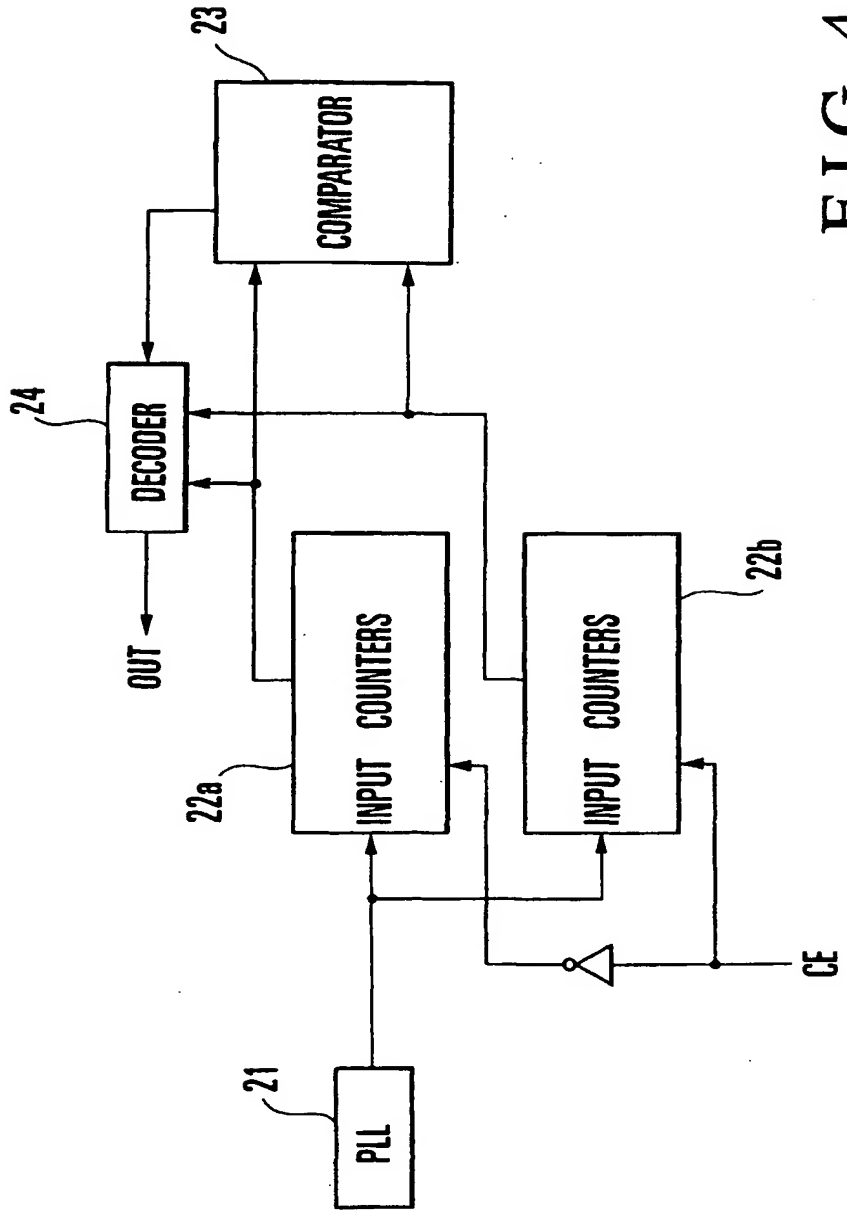
23
COMPARATOR
24
DECODER
OUT
22a
INPUT COUNTERS
22b
INPUT COUNTERS
CE
21
PLL

FIG. 4

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(71) Applicant: **NEC Electronics Corporation**
Kawasaki, Kanagawa 211-8668 (JP)

(72) Inventor: **Yamaguchi, Michimasa,**
c/o NEC IC Microcomputer
Kawasaki-shi, Kanagawa (JP)

(74) Representative: **Betten & Resch**
Postfach 10 02 51
80076 München (DE)

(54) Frequency measurement test circuit and semiconductor integrated circuit having the same

(57) A frequency measurement test circuit includes a frequency divider (1), and a detection circuit. The frequency divider frequency-divides an input to be measured. The detection circuit outputs a signal of level set on the basis of a relationship in magnitude between the frequency of the signal frequency-divided by the frequency divider and that of a reference clock signal.

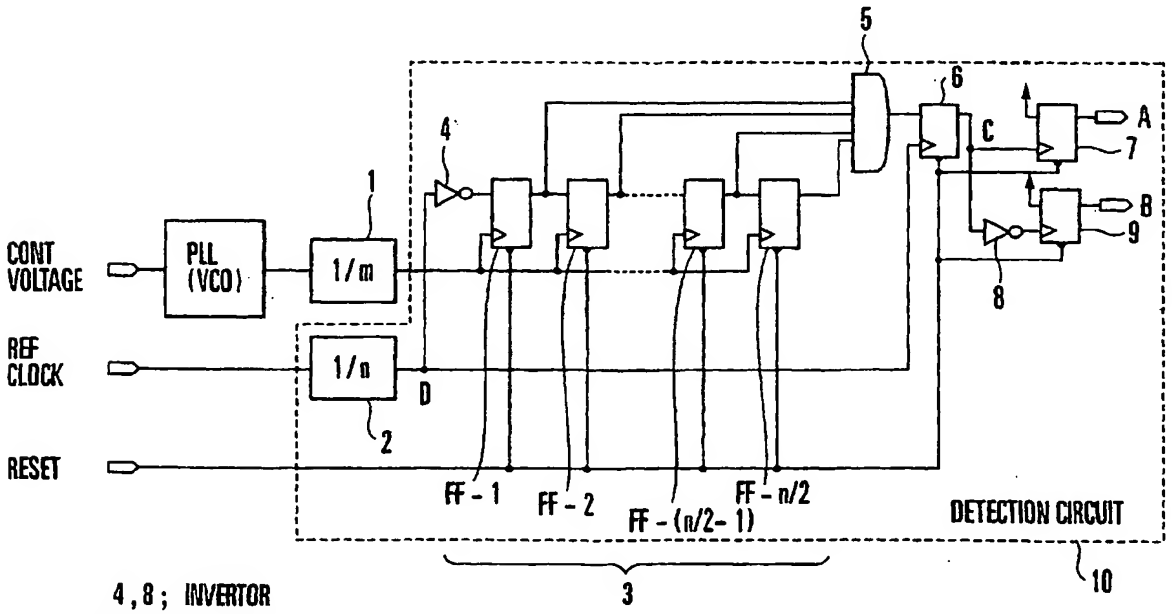

FIG. 1

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Application Number
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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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G01R

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	25 September 2003	Binger, B

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X : particularly relevant if taken alone
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EPO FORM 1503 03.82 (P04C01)

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